Flash In_2Se_3 for neuromorphic computing

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Abstract:

The development of next-generation in-memory and neuromorphic computing can be realized with memory transistors based on two-dimensional (2D) ferroelectric semiconductors. Among these, In_2Se_3 is the most interesting since it possesses ferroelectricity in 2D quintuple layers. However, synthesis of large amounts of In_2Se_3 crystals with the desired phase has not been previously achieved. We demonstrate here the gram-scale synthesis of α-In_2Se_3 crystals using a flash-within-flash Joule heating method. This approach allows the synthesis of single-phase α-In_2Se_3 crystals regardless of the conductance of precursors in the inner tube and enables the

synthesis of gram-scale quantities of α-In_2Se_3 crystals. We then fabricate and use α-In_2Se_3 flakes as a 2D ferroelectric semiconductor FET artificial synaptic device platform. By modulating the degree of polarization in α-In_2Se_3 flakes according to the gate electrical pulses, these devices exhibit distinct essential synaptic behaviors. Their synaptic performances show excellent and robust reliability under repeated electrical pulses. Finally, we demonstrate that the synaptic devices achieve an estimated learning accuracy of up to ~87% for Modified National Institute of Standards and Technology patterns in a single-layer neural network system.

Keywords flash-within-flash Joule heating, α-In_2Se_3, flash Joule heating, ferroelectricity, neuromorphic applications

Main Text:

Two-dimensional (2D) semiconductors with inherent polarization direction based on homostructures or heterostructures offer numerous advantages for distinct electronic applications, including diode,[1–4] photodiode,[5–7] ferroelectric field-effect transistor (Fe-FET),[8–11] in-memory computing,[12–14] and neuromorphic applications.[15–17] Due to their atomically thin thickness and inherent polarization properties, the 2D Fe-FET have the potential for higher integration density in electronic circuits and integrated logic and memory functions with low energy consumption, surpassing conventional von Neumann computing architecture.[18] Among the various reported 2D ferroelectric materials, such as In_2Se_3,[19] SnSe,[20] $MoTe_2$,[21] and SnS,[22] α-In_2Se_3 stands out with its appropriate bandgap (-1.39 eV), and room-temperature out-of-plane and in-plane ferroelectric characteristics with the Curie temperature >200 °C, even down to the monolayer limit.[19]

Bottom-up synthetic methods, such as chemical-vapor deposition (CVD),[23] physical vapor deposition (PVD),[24] molecular beam epitaxy (MBE),[12] and pulsed laser deposition (PLD),[25] have

been used to synthesize atomically thin In_2Se_3 layers. For example, the CVD methods have been intensively investigated and demonstrated to grow large-area 2D In_2Se_3 films. However, due to the complicated polymorphism and low phase-transition temperature between In_2Se_3 phases, it is difficult to synthesize pure-phase In_2Se_3 films.[26] In addition, bottom-up strategies for producing high-quality In_2Se_3 are often restricted to ultrasmall amounts. Recently, flash Joule heating (FJH) has been demonstrated as an effective method for producing gram-scale flash graphene from various carbon feedstocks,[27–30] kilogram scales in automated FJH laboratory system,[31] and ton-scales in industry (www.universalmatter.com). Contrary to the conventional bottom-up synthetic methods, FJH provides short electrical pulses of high energy density followed by rapid cooling that can generate products within milliseconds to seconds with high energy efficiency.[27] Moreover, FJH can be used for phase control of transition metal dichalcogenides (TMD),[32,33] heteroatom doped-graphene,[34] and turbostratic-layered 2D materials.[35] However, a significant limitation of FJH is that for Joule heating to occur, the precursors should have a resistivity below a certain level (0.5 – 30 Ω). To solve this requirement, carbon additives or metal powders are mixed into the precursors to generate a conducting path for electrical current, facilitating the reaction.[27] However, these additives can generate undesired byproducts, often the metal(0) or metal carbide.[36]

To overcome this limitation of FJH, our group recently developed a method called flash-within-flash Joule heating (FWF) to achieve indirect heating, enabling non-conductive precursors to undergo flashing through thermal conduction.[37] In this study, we present the synthesis of pure α-In_2Se_3 crystals by employing the FWF. This method allows us to produce single-phase α-In_2Se_3 crystals even if the precursor in the inner tube is non-conductive, thereby generating α-In_2Se_3 crystals on the gram-scale. Moreover, we fabricated and used ferroelectric semiconductor FET (FS-FET) devices with α-In_2Se_3 flakes as a 2D FS-FET artificial synaptic device platform. They

exhibit the distinct essential synaptic behaviors through careful modulation of the degree of polarization of the α-In_2Se_3 flakes, depending on the gate-electrical stimulus. In addition, their synaptic performances show excellent and robust reliability under repeated electrical pulses. Finally, we demonstrated that the estimated learning accuracy of our synaptic devices is up to ~87% for Modified National Institute of Standards and Technology (MNIST) patterns in a single-layer neural network system.

FWF process and α-In_2Se_3 crystals characterization

Fig. 1a exhibits the schematic diagram of FWF synthesis process as an indirect Joule heating mechanism that allows the feedstocks of indium (In) pellets and selenium (Se) powder to be reacted rapidly within 3 s. The reaction occurs in two quartz tubes: an outer flashing vessel filled with a conductive material, such as metallurgical coke, and an inner flashing vessel that contains the feedstocks of In(0) and Se(0). The inner flashing vessel was filled by In pellets and Se powder with molar ratio of 1:3, and we applied the flashing voltage of 300 V to the outer vessel to generate the Joule heating process. **Fig. 1**b exhibits the current profiles during the flashing process in the FWF system. While the current passes through the conductive feedstocks in the outer vessel, resistive Joule heating generates a high temperature of >2,000 °C in the outer vessel, as measured by an infrared sensor (**Fig. S**1). Since the discharge is pulsed at different duty cycles of 10%, 20%, and 50% (**Fig. S**2), a constant reaction temperature, pressure, and volume is not achieved during the flashing, leading to a kinetically assisted synthetic process during the FWF method. Based on a Gibbs free energy calculation, an energy favorable reaction can be achieved in the range of the temperature during the flashing, meaning that the synthesis of In_2Se_3 is feasible by the FWF method (**Fig. S**3). Moreover, the metallurgical coke in the outer vessel is converted

into the turbostratic flash graphene after the FWF reaction, consistent with the gram-scale graphene synthesis studies (**Fig. S**4).[27,31]

To verify the physical characteristics of the inner tube products from FWF synthesis process, we conducted transmission electron microscopy (TEM), X-ray diffraction (XRD), X-ray photoelectron spectroscopy (XPS), and Raman spectroscopy measurements. **Fig. 1**c exhibits the annual dark-field scanning transmission electron microscopy (ADF-STEM) images of α-In_2Se_3 crystals with highly crystalline structure, and corresponding Fourier transform shown in the inset of **Fig. 1**c. In addition, the elemental compositions of the flakes are investigated by energy dispersive spectrometer (EDS) mapping (**Fig. S**5). From the results, the synthesized flakes are confirmed to be composed of pure In and Se elements. **Fig. 1**d exhibits the XRD pattern of the as-prepared powders. All the diffraction peaks correspond to the hexagonal α-In_2Se_3 phase (DB card number: 00-034-1279) with hexagonal $P6_3mc$ crystalline structure. In the Raman spectra shown in **Fig. 1**e, the representative A_1^1, E^4, and A_1^2 vibrational modes are observed at 105, 181, and 193 cm^{-1}, respectively, confirming α-phase In_2Se_3 flakes.[38] XPS was also conducted to confirm the atomic composition of the flakes (**Fig. 1**f). From the full-scan XPS spectrum (**Fig. S**6), the spectral characteristic peaks clearly indicate the formation of In_2Se_3. The 3d doublets of In and Se clearly demonstrate the chemical valence of In and Se in In_2Se_3 flakes. The negligible C and O signals of are presumably from the atmosphere. Moreover, when scaling up to gram-scale the α-In_2Se_3 retains its high purity and single-phase structure while the synthesis time remains within 3 s (**Fig. S**7). Hence, the gram-scale synthesis of α-In_2Se_3 crystals by the FWF method was confirmed to afford a single phase with high crystallinity.

Electrical characteristics of flashed α-In_2Se_3 FET devices

To investigate the electrical characteristics of as-prepared α-In_2Se_3 flakes by FWF, a FET with α-In_2Se_3 flakes was fabricated. **Figs. 2**a-b exhibit an optical microscope image and device schematic of the α-In_2Se_3 FET device, where the FET device consists of a SiO_2 (285 nm)/Si (heavily p-doped) substrate as a backgate configuration, 2D α-In_2Se_3 flakes as the ferroelectric semiconductor channel and 10 nm Ti/50 nm Au as source/drain electrode contacts. The details of the device fabrication procedure are discussed in the Methods section and Supplementary Information (**Fig. S**8). As shown in **Fig. 2**c, the individual layers of α-In_2Se_3 are distinct in the cross-sectional high-resolution ADF-STEM image, indicating that the α-In_2Se_3 FET devices are cleanly fabricated without noticeable damage of the interlayer and electrode contacts. **Figs. 2**d and g exhibit representative output (drain voltage (V_D)-drain current (I_D) characteristics depending on various gate voltage (V_G)) and transfer curve (V_G-I_D characteristics depending on various V_D) for the α-In_2Se_3 FET device, respectively, and show the typical *n*-type semiconducting behavior (**Fig. S**9) with a channel current ON/OFF ratio of $>10^4$.[8] Since the α-In_2Se_3 is highly light sensitive, we measured the electrical characteristics under dark conditions (**Figs. S**10-11). Moreover, the gate double sweep from -40 to 40 V for 100 cycles was conducted to investigate the device stability under repetitive electric stimuli (**Fig. S**12). After 100 cycles of electrical stimuli, the transfer curve of 100th sweep is almost identical with that of 1st sweep, meaning that the devices are very stable and robust under repetitive electrical stimuli. In addition, a large clockwise hysteresis is observed when the V_G is double swept between -40 and 40 V at a fixed V_D of 0.1 (black), 1.0 (red), and 2.0 V (blue) in **Fig. 2**e, indicating that the device can exhibit a memory operation under V_G sweep.[8,13,15,39] In addition, the hysteresis memory window can be tuned by using different gate sweep ranges (**Fig. 2**h). When the gate sweep range becomes larger, the hysteresis window can be larger from 7.5 V under V_G sweep of -10 to 10 V to 38.5 V under V_G sweep of -40 to 40 V (**Fig.**

2e), indicating that the polarization can be precisely controlled by adjusting the electric field. This results because the degree of polarization of In_2Se_3 can be stronger when the gate electric field is increased, leading to larger hysteresis memory window. Therefore, the device can exhibit two distinct electrical states after V_G is turned off, i.e., ON current state (ON) and OFF current state (OFF). The ratio between the two electrical states is ~10^2, indicative of a large dynamic range. **Fig. 2**f exhibits the retention test for 5×10^2 s, however, ON and OFF states were degraded after 10^2 s. Since the electron transfer direction and inherent polarization direction are perpendicular to each other, the mobile charge can disrupt the polarization direction, leading to degradation of ON and OFF states.[40,41] **Fig. 2**i exhibits the endurance test of our device by executing 10^3 repetitive pulse schemes (**Fig. S**13) with ON-OFF ratio of $<10^2$. Unlike the retention test, the endurance characteristics were stable and robust for 10^3 cycles, so the device could be operated with stability under repetitive writing and erasing.

Ferroelectric switching mechanism

To understand the hysteresis phenomenon in α-In_2Se_3 FET devices, an energy band diagram at the two polarization states (up and down) is employed after $V_G < 0$ or $V_G > 0$ was applied (**Fig. 3**a). When the high negative V_G was applied, the inherent electric field in α-In_2Se_3 was formed to downward direction.[8,19] Consequently, the positive-bound charges near the interface between α-In_2Se_3 and SiO_2 is produced, leading to energy band downshift. In contrast, when the high positive V_G was applied, the polarization of α-In_2Se_3 was formed to upward direction, inducing that negative-bound charges near the interface between α-In_2Se_3 and SiO_2 is produced and energy band of α-In_2Se_3 can be downshifted.[8,19] The polarization characteristics can be maintained even when the V_G was turned off due to the ferroelectric characteristics of α-In_2Se_3.

Therefore, the α-In_2Se_3 FET device can exhibit non-volatile memory characteristics with ON and OFF states after $V_G < 0$ and $V_G > 0$, respectively. The details are discussed in Methods section.

Synaptic behavior of flashed α-In_2Se_3 FS-FET devices

The α-In_2Se_3 FS-FET artificial synapse can implement two essential synaptic functions distinguished by a temporal or persistent change in the synaptic weight: (i) short-term plasticity (STP) and (ii) long-term plasticity (LTP). **Fig. 3**b shows the post-synaptic current (I_{PSC}) changes over time generated by different single presynaptic pulses of V_G = -40 V with pulse widths (w) of 10 ms (black), 100 ms (red), and 1 s (blue) at V_D = 1 V. When the shorter w (V_G = -40 V for 10 ms) was applied to the preneuron (gate electrode), the I_{PSC} was temporally changed, i.e., its value returned to the original one. This I_{PSC} behavior is analogous to the STP of the biological synapse, which is excited for only a short period. In contrast, when the longer w (V_G = -40 V for 1 s) was applied to the preneuron, the I_{PSC} increased abruptly from 4.53×10^{-10} to 1.61×10^{-9} A, and then regained their electrical state for a longer period. Note that the temporal current drop before increasing the current originates from the gate-electric field effect. This I_{PSC} behavior is analogous to the LTP that represents memory consolidation in the brain. The V_G pulses for increasing I_{PSC} is called the potentiating pulse.

A longer V_G (-40 V for 1 s) can sufficiently upward-polarize the domain in the α-In_2Se_3 to the direction of the SiO_2 gate dielectric layer compared with a shorter V_G (-40 V for 10 ms). Therefore, the electrons can accumulate at the interface between the α-In_2Se_3 and SiO_2 layer, increasing the electrical current states and retaining it for a long time. The LTP can be mimicked because the accumulated electrons at the interface are retained to some extent owing to the remnant upward polarization. Considering the similarity of the operation to a biological synaptic cleft, the

upward polarization degree can be regarded as the quantity of the neurotransmitters released and the concentration of the Ca^{2+} influx into the axon terminal of the preneuron, respectively.[42]

The synaptic weight can also be controlled by changing the number of preneuron voltage pulses applied in a given time; that is, the degree of the I_{PSC} increases can be affected by the time interval (Δt) between two potentiating pulses. **Fig. 3**c shows the I_{PSC} changes for 20 repeated pulses (V_G = -40 V for 100 ms) depending on different Δt (0.1 (black), 1 (red), and 8 s (blue), respectively). A shorter Δt (0.1 s) led to a larger and more rapid increase in the I_{PSC}. This results because the potentiating pulses with a shorter Δt further induced the upward domain of polarization before the postsynaptic responses to the previous pulse was completely attenuated, leading to strengthen and retaining the degree of polarization in α-In_2Se_3 crystals. In contrast, the longer Δt (8 s) could fully attenuate the response; hence the final I_{PSC} was barely changed. This Δt dependency on the I_{PSC} is like the phenomenon of temporal summation of the signal propagation that occurs when the input graded potentials from one biological preneuron are close together over a given time. This is regarded as one of the main features of the spike rate-dependent plasticity (SRDP).[43] Since higher absolute values of input pulses can further change the direction of polarization, the dynamic range of I_{PSC} can also be increased as the V_G increased from ±10 to ±40 V (**Fig. S**14).

Fig. 3d shows the gradual LTP and long-term depression (LTD) of I_{PSC} depending on the continuous potentiating and depressing input pulse trains. When the polarity of the presynaptic pulse is changed from negative to positive, the direction of polarization is changed to the opposite, which can repel the accumulated electrons and deplete the interfacial region. Consequently, the I_{PSC} gradually decreases during the positive depressing input pulse train. This gradual I_{PSC} reduction is analogous to the LTD of a biological synapse.[42] For practical and robust neuromorphic device applications, stable synaptic functions under repeated pulse cycles are essential. **Fig. 3**e

shows the repetitive transitions between LTP/LTD functions over 4,000 continuous input pulses. The number of presynaptic pulses for one cycle was 40, each consisting of 20 potentiating pulses (V_G = -40 V for 100 ms) and 20 depressing pulses (V_G = 20 V for 100 ms), demonstrating stable repetitive LTP/LTD functions over the 4,000 electrical pulses. Furthermore, the I_{PSC} values for the first (red) and last three cycles (blue) were almost identical (**Fig. 3**f). These stable synaptic functions under repeated pulse cycles were demonstrated under V_G = ±10, ±20, and ±30 V, respectively, where the electrical characteristics are stable and robust regardless of the operating voltage amplitudes (**Figs. S**15-**S**17). This indicates the reproducibility and robust control of the synaptic weight with very stable operation even over 4,000 electrical pulses.

MNIST pattern recognition simulation

To evaluate the learning capability of the α-In_2Se_3 FS-FET device (**Fig. 4**a) to be a constituent as a synaptic weight element in tri-synaptic artificial neural network for neuromorphic applications, we prepared an unstructured data set and single-layer neural network platform to adjust the analog conductance of the device and to update the synaptic weights (**Fig. 4**b). We simulated the training and test process using 20-level analog switching characteristics of the α-In_2Se_3 FS-FET device in the influence of different gate voltage (10, 20, 30, and 40 V) for the conventional binary MNIST digit image set (60,000 training and 10,000 test set).[44] Here, the test set was prepared differently from the training set to identify the availability of the formed 10 × 28 × 28 synaptic weight map for recognizing the correct output class. The 10-class (0, 1, 2, …, 9) MNIST datasets contain images of 28 × 28 pixels represented by binary resolution and are further determined by pixel brightness (black and white pixels). The training principle of the neuromorphic perceptron process is provided in the Supplementary Note 1. **Fig. 4**c shows

classification accuracy during 30 training processes at gate voltage of 10 V. As the training epoch increases, the accuracy value is evolved to converge to ~87%, which is near the ideal single-layer accuracy of ~88% using numerical weight values excluding device parameters. The classification accuracy for different operating voltages (V_G = 20, 30, and 40 V) is 86.77, 86.36, and 86.02%, respectively (**Fig. S**18).[44,45] **Fig. 4**d shows the confusion matrix of 10,000 test images after the 30-training epoch at a gate voltage of 10 V. Here, the row indicates recognized classes, and the column indicates the actual classes. The ratio of summation of diagonal elements to the entire 10,000 images shows recognition accuracy of ~87%. Based on these results, the single-neural network based on the α-In_2Se_3 FS-FET device properly and accurately performs the learning and recognition tasks.

Conclusion

In conclusion, highly crystalline and single-phase α-In_2Se_3 was successfully synthesized by the FWF reaction, and the materials characteristics were analyzed by XRD, XPS, EDS, TEM, and Raman analysis. Based on as-synthesized α-In_2Se_3 with single phase and high crystallinity, the α-In_2Se_3 synaptic devices were successfully fabricated. Diverse and well-defined synaptic functions, including STP, LTP/LTD, and SRDP, were demonstrated. In addition, the transitions between the LTP/LTD functions were stable under repeated pulse cycles regardless of operating voltage amplitude. Notably, the α-In_2Se_3 synaptic devices achieved up to ~87% recognition accuracy for MNIST patterns, even in a single-layer neural network system. The results indicate that our α-In_2Se_3 with single phase and high crystallinity synthesized by FWF can hold the advantages of simple, fast, and gram-scalability, as well as well-defined electrical and synaptic functions.

References

1. Lee, C.-H. *et al.* Atomically thin p-n junctions with van der Waals heterointerfaces. *Nat. Nanotechnol.* **9**, 676–81 (2014).

2. Shin, J. *et al.* Tunable rectification in a molecular heterojunction with two-dimensional semiconductors. *Nat. Commun.* **11**, 1412 (2020).

3. Zhang, X. *et al.* Near-ideal van der Waals rectifiers based on all-two-dimensional Schottky junctions. *Nat. Commun.* **12**, 1522 (2021).

4. Eo, J. S. *et al.* Tailoring the interfacial band offset by the molecular dipole orientation for a molecular heterojunction selector. *Adv. Sci.* **8**, e2101390 (2021).

5. Mennel, L. *et al.* Ultrafast machine vision with 2D material neural network image sensors. *Nature* **579**, 62–66 (2019).

6. Shin, J. *et al.* Molecular van der Waals heterojunction photodiodes enabling dipole-induced polarity switching. *Small Methods* **6**, e2200646 (2022).

7. He, T. *et al.* On-chip optoelectronic logic gates operating in the telecom band. *Nat. Photonics* 1–8 (2023) doi:10.1038/s41566-023-01309-7.

8. Si, M. *et al.* A ferroelectric semiconductor field-effect transistor. *Nat. Electron.* **2**, 580–586 (2019).

9. Tan, C. *et al.* 2D fin field-effect transistors integrated with epitaxial high-k gate oxide. *Nature* **616**, 66–72 (2023).

10. Jiang, J., Xu, L., Qiu, C. & Peng, L.-M. Ballistic two-dimensional InSe transistors. *Nature* **616**, 470–475 (2023).

11. Mondal, A. *et al.* Low Ohmic contact resistance and high on/off ratio in transition metal dichalcogenides field-effect transistors via residue-free transfer. *Nat. Nanotechnol.* 1–10 (2023) doi:10.1038/s41565-023-01497-x.

12. Poh, S. M. *et al.* Molecular-beam epitaxy of two-dimensional In_2Se_3 and its giant electroresistance switching in ferroresistive memory junction. *Nano Lett.* **18**, 6340–6346 (2018).

13. Li, X. *et al.* Multi-functional platform for in-memory computing and sensing based on 2D ferroelectric semiconductor α-In_2Se_3. *Adv. Funct. Mater.* (2023) doi:10.1002/adfm.202306486.

14. Huang, X. *et al.* An ultrafast bipolar flash memory for self-activated in-memory computing. *Nat. Nanotechnol.* **18**, 486–492 (2023).

15. Wang, L. *et al.* Exploring ferroelectric switching in α-In_2Se_3 for neuromorphic computing. *Adv. Funct. Mater.* **30**, (2020).

16. Liu, K. *et al.* An optoelectronic synapse based on α-In_2Se_3 with controllable temporal dynamics for multimode and multiscale reservoir computing. *Nat. Electron.* **5**, 761–773 (2022).

17. Li, T. *et al.* Reconfigurable, non-volatile neuromorphic photovoltaics. *Nat. Nanotechnol.* 1–8 (2023) doi:10.1038/s41565-023-01446-8.

18. Kim, K.-H. *et al.* Scalable CMOS back-end-of-line-compatible AlScN/two-dimensional channel ferroelectric field-effect transistors. *Nat. Nanotechnol.* **18**, 1044–1050 (2023).

19. Ding, W. *et al.* Prediction of intrinsic two-dimensional ferroelectrics in In_2Se_3 and other III2-VI3 van der Waals materials. *Nat. Commun.* **8**, 14956 (2017).

20. Luo, Y. *et al.* Electrically switchable anisotropic polariton propagation in a ferroelectric van der Waals semiconductor. *Nat. Nanotechnol.* **18**, 350–356 (2022).

21. Hou, W. *et al.* Strain-based room-temperature non-volatile $MoTe_2$ ferroelectric phase change transistor. *Nat. Nanotechnol.* **14**, 668–673 (2018).

22. Higashitarumizu, N. *et al.* Purely in-plane ferroelectricity in monolayer SnS at room temperature. *Nat. Commun.* **11**, 2428 (2020).

23. Han, W. *et al.* Phase-controllable large-area two-dimensional In_2Se_3 and ferroelectric heterophase junction. *Nat. Nanotechnol.* **18**, 55–63 (2022).

24. Zhou, J. *et al.* Controlled synthesis of high-quality monolayered α-In_2Se_3 via physical vapor deposition. *Nano Lett.* **15**, 6400–5 (2015).

25. Chanchal, Jindal, K., Pandey, A., Tomar, M. & Jha, P. K. Phase-defined growth of In_2Se_3 thin films using PLD technique for high performance self-powered UV photodetector. *Appl. Surf. Sci.* **595**, 153505 (2022).

26. Tao, X. & Gu, Y. Crystalline-crystalline phase transformation in two-dimensional In_2Se_3 thin layers. *Nano Lett.* **13**, 3501–5 (2013).

27. Luong, D. X. *et al.* Gram-scale bottom-up flash graphene synthesis. *Nature* **577**, 647–651 (2020).

28. Wyss, K. M. *et al.* Converting plastic waste pyrolysis ash into flash graphene. *Carbon* **174**, 430–438 (2021).

29. Advincula, P. A. *et al.* Flash graphene from rubber waste. *Carbon* **178**, 649–656 (2021).

30. Wyss, K. M. *et al.* Upcycling end-of-life vehicle waste plastic into flash graphene. *Commun. Eng.* **1**, 3 (2022).

31. Eddy, L. *et al.* Laboratory Kilogram-scale graphene production from coal. (2023) doi:10.26434/chemrxiv-2023-7z1s2.

32. Chen, W. *et al.* Millisecond conversion of metastable 2D materials by flash Joule heating. *ACS Nano* **15**, 1282–1290 (2021).

33. Chen, W. *et al.* Ultrafast and controllable phase evolution by flash Joule heating. *ACS Nano* **15**, 11158–11167 (2021).

34. Chen, W. *et al.* Heteroatom-Doped Flash Graphene. *ACS Nano* **16**, 6646–6656 (2022).

35. Chen, W. *et al.* Turbostratic boron–carbon–nitrogen and boron nitride by flash Joule heating. *Adv. Mater.* **34**, e2202666 (2022).

36. Deng, B. *et al.* Phase controlled synthesis of transition metal carbide nanocrystals by ultrafast flash Joule heating. *Nat. Commun.* **13**, 262 (2022).

37. Choi, C. *et al.* Flash-within-flash synthesis of gram-scale solid-state materials. (2023) doi:10.26434/chemrxiv-2023-h2nph.

38. Lewandowska, R., Bacewicz, R., Filipowicz, J. & Paszkowicz, W. Raman scattering in α-In2Se3 crystals. *Mater. Res. Bull.* **36**, 2577–2583 (2001).

39. Wan, S. *et al.* Nonvolatile ferroelectric memory effect in ultrathin α-In_2Se_3. *Adv. Funct. Mater.* **29**, (2019).

40. Ma, T. P. & Han, J.-P. Why is nonvolatile ferroelectric memory field-effect transistor still elusive? *IEEE Electron Device Lett.* **23**, 386 (2002).

41. Yurchuk, E. *et al.* Charge-trapping phenomena in HfO_2-based FeFET-type nonvolatile memories. *IEEE Trans. Electron Devices* **63**, 3501–3507 (2016).

42. Dodge, F. A. & Rahamimoff, R. Co-operative action of calcium ions in transmitter release at the neuromuscular junction. *J. Physiol.* **193**, 419–432 (1967).

43. Rachmuth, G., Shouval, H. Z., Bear, M. F. & Poon, C.-S. A biophysically-based neuromorphic model of spike rate- and timing-dependent plasticity. *Proc. Natl. Acad. Sci.* **108**, E1266–E1274 (2011).

44. Deng, L. The MNIST database of handwritten digit images for machine learning research [best of the web]. *IEEE Signal Process. Mag.* **29**, 141–142 (2012).

45. Kwak, T. *et al.* Ultra-large dynamic range synaptic indium gallium zinc oxide transistors. *Appl. Mater. Today* **29**, 101648 (2022).

Methods

Materials synthesis

In metal pellets (0.42 g) and Se powder (0.84 g) were placed inside the 8 mm quartz tube with graphite spacer and copper mesh at each end of the quartz tube. Only graphite spacers were in contact with the metal precursors. This tube is then placed inside the 15 mm quartz tube and is subsequently filled with metallurgical coke (5.0 g). The copper mesh and graphite spacer were also placed at each end of the outer quartz tube. The combined tubes were flash-Joule-heated using 300 V, and the products from FJH were collected without further purification and washing. For gram-scale synthesis, In metal pellet (0.84 g) and Se powder (2.15 g) were placed inside the 8 mm quartz tube with graphite spacer and copper mesh at each end of the quartz tube, and FWF system was made with the same procedure. The combined tubes were flash-Joule-heated using 260 V, and the products from FJH were collected without further purification and washing.

Material characterization

Materials characterization of α-In_2Se_3 were carried out to investigate α-In_2Se_3, as a single-crystal semiconducting and ferroelectric material, including STEM, Raman spectroscopy, XPS, and XRD. STEM images were collected on a FEI Titan Themis S/TEM system operating at 300 keV. The powder samples were prepared by drop-casting a 300-μL aliquot (1 mg of sample/1 mL ethanol) on Cu/lacey carbon TEM grid (Ted Pella). The resultant grid was dried at 80 °C on a hotplate for 1 h with subsequent overnight vacuum drying. For cross-sectional TEM images, focused ion beam (FIB) cutting was performed with FEI Helios NanoLab 660 DualBeam system. The resultant FIB cross-section sample was attached to PELCO® Cu half grids (Ted Pella) for further characterization under ADF-STEM. Raman spectra were obtained using a Renishaw Raman

microscope (532 nm laser, 50× lens) with the exfoliated α-In_2Se_3 flakes on SiO_2/Si substrate. XPS were obtained using PHI Quantera SXM Scanning X-ray Microprobe with a base pressure of 5 × 10^{-9} Torr. All XPS spectra were corrected using carbon 1s (284.8 eV) peak as a reference. XRD spectra were collected using Rigaku SmartLab XRD with CuKα radiation from 2θ angle of 3° to 80° with the scan rate of 10 °/min.

Device fabrication

The α-In_2Se_3 samples were prepared using typical mechanical exfoliation methods on SiO_2 (285 nm)/Si substrate, respectively. Briefly, as-prepared α-In_2Se_3 flakes were placed between two pieces of adhesive tape and then pulled off very carefully to make thinner layers of α-In_2Se_3. After repeating this process 5 times, the adhesive tape is pressed onto the SiO_2 substrate and gently rubbed for 2 min. And then the adhesive tape was gently pulled off. The thickness of the layers was estimated by optical contrast. Cross-sectional TEM was used to determine their thicknesses. To make electrical contact, conventional photolithography was used to make the source and drain patterns where the channel length is 3 μm, and 10 nm of Ti and 50 nm of Au metal were deposited by an electron beam evaporator under a pressure of ~10^{-8} Torr and deposition rate of 2.0 Å/s. To remove the residual photoresist, the sample was immersed in an acetone bath for 6 ~ 12 h, and then the solution was gently blown by a stream of N_2 gas. Finally, to enhance the interfacial contact properties between metal/2D materials, the fabricated devices were stored for 6 ~ 12 h under vacuum (~10^{-3} Torr) conditions. The processes used to fabricate the devices are schematically shown in Supplementary Information (**Fig. S**8).

Device characterization

The electrical characteristics were measured with a semiconductor parameter analyzer (Agilent B1500A Semiconductor Device Analyzer) and a probe station system in the dark to avoid the generation of photo-excited electrons and holes in 2D materials. The source electrode was grounded, the drain voltage was applied by the drain electrode, and the Si substrate was used as the backgate electrode. The measurement was conducted under high vacuum condition (~10^6 Torr)

Surface treatment and measurement condition

It is known that multiple factors can result in clockwise gate hysteresis on transistors made from layered semiconductors, such as absorption of water and oxygen molecules, interfacial charge states, and even intrinsic material defects. In this work, we verify that the hysteresis is attributed to the inherent ferroelectric characteristics of α-In_2Se_3 flakes based on a series of experimental conditions. The electrical measurements were conducted under high vacuum, where the contribution of surface adsorbates including water and oxygen molecules can be minimized. Moreover, H_2 and O_2 plasma treatments were applied onto the SiO_2/Si substrate before α-In_2Se_3 flakes exfoliation to remove the dangling bonds on the SiO_2 surface, mitigating the contribution of interface-trap-induced hysteresis. Therefore, the clockwise hysteresis and memory characteristics of our devices originate from the inherent ferroelectricity of α-In_2Se_3.

MNIST pattern recognition simulation

The MNIST pattern recognition simulation is based on the results of LTP and LTD in **Fig. 3** and was carried out to investigate the learning capability of the α-In_2Se_3 FET synaptic devices. This single-layer artificial neural network consists of 784 input neurons (28 × 28 pixels) and 10 output

neurons with full connection by an individual synapse that has its own synaptic weight. The details of MNIST pattern recognition simulation are discussed in Supplementary Note 1.

Flash Joule Heating Equipment

The flash Joule heating reactions were performed by a custom-built system using capacitor banks to deliver the flash. 48 Kemet ALS70A133QT500 capacitors, each rated at 13 mF and 500 V, were connected in parallel (624 mF total) and charged to the desired voltage. A variable frequency driver controlled the discharge intensity using pulse width modulation by using a duty cycle pattern operating at 1 kHz of 10% intensity for 1 s, followed by 20% for 0.5 s, and finally 50% for 5 s. It should be noted that almost all the voltage is used during the 10% and 20% duty cycle; the 50% duty cycle is to ensure all the voltage is discharged through the sample. The duty cycles, charging, and flashing operations were controlled by a custom LabVIEW program. The current discharged during flashing was measured using a Tamura L34S1T2D15 Hall effect sensor. The temperature was measured using a Micro-Epsilon CTRM1H1SF100-C3 pyrometer.

Online content

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Author contributions

J.S. conceived with the device idea with C.H.C. and L.E., realized the demonstration of synthesizing In_2Se_3 materials by flash-within-flash Joule heating, conducted gram-scalability, XRD, XPS, Raman, electrical measurements, artificial neuromorphic measurements, and manuscript writing under the guidance of J.M.T.; J.J. performed MNIST pattern recognition simulation; C.H.C. performed STEM and EDS characterization; L.E. managed the FJH system; P.S. aided Raman spectroscopy analysis; Y.H. supervised C.H.C. in performing STEM and EDS characterization. J.M.T. supervised J.S. for all the process, guided J.S. in manuscript writing, and oversaw the entire project.

Competing interests

Rice University own intellectual property (IP) surrounding the concepts in this manuscript. That IP is presently unlicensed.

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Figure 1

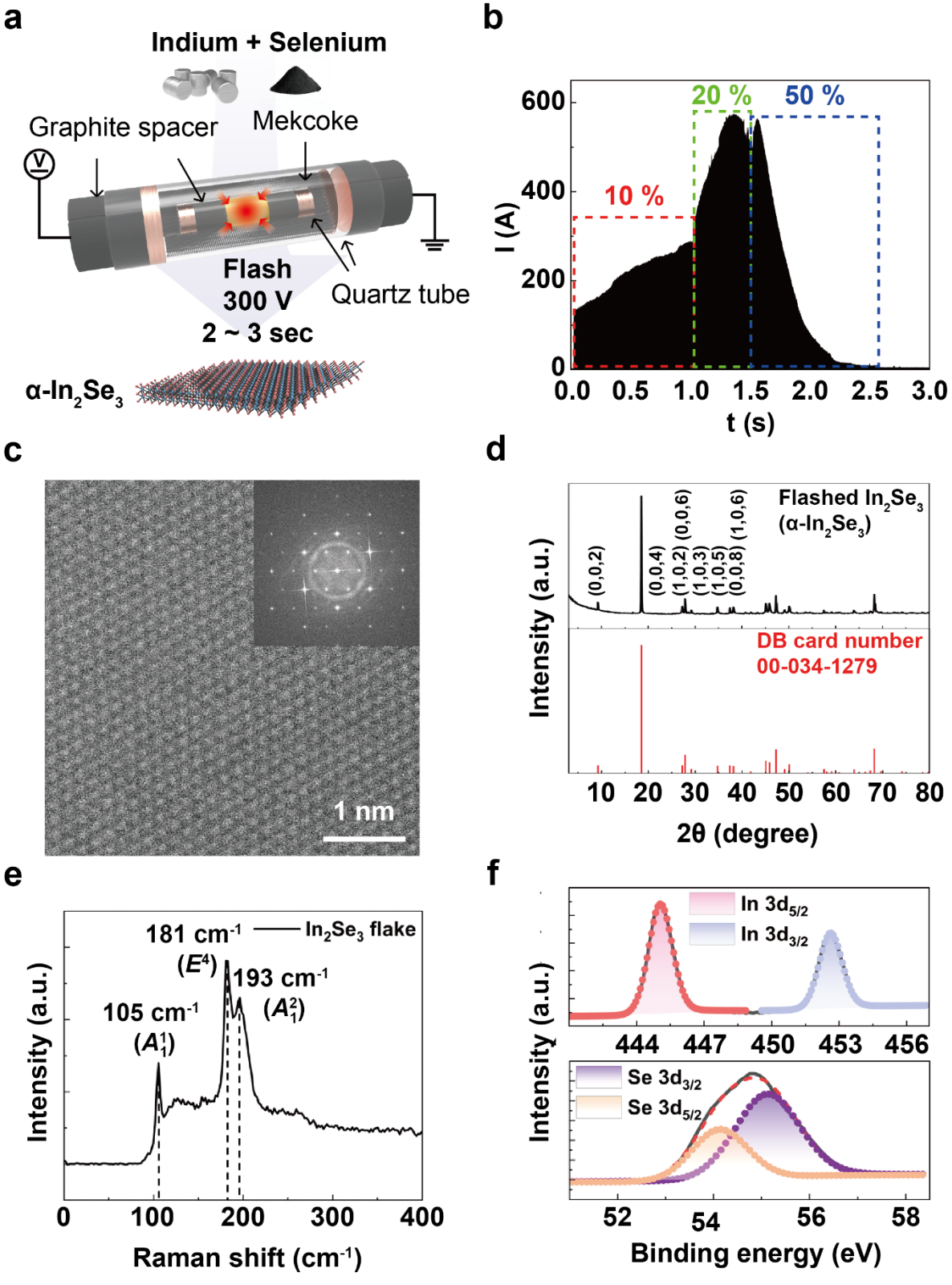

Figure 1. A α-In_2Se_3 synthesis by flash-within-flash Joule heating (FWF) and materials characteristics. a, A schematic of FWF with the precursors of In metal pellets and Se powder forming α-In_2Se_3. **b,** The current profile of 300 V FWF reaction. The dashed boxes indicate the regions of different duty cycles (10% (red), 20% (green), and 50% (blue)). **c,** Annular dark field STEM image and Fourier transform (inset) of α-In_2Se_3 powder **d,** XRD spectra of α-In_2Se_3 with R3m crystalline structure. **e,** Raman spectrum of α-In_2Se_3 with typical Raman peaks of 105, 181, and 193 cm^{-1}. **f**, XPS of α-In_2Se_3 for In (top) and Se (bottom) atoms.

Figure 2

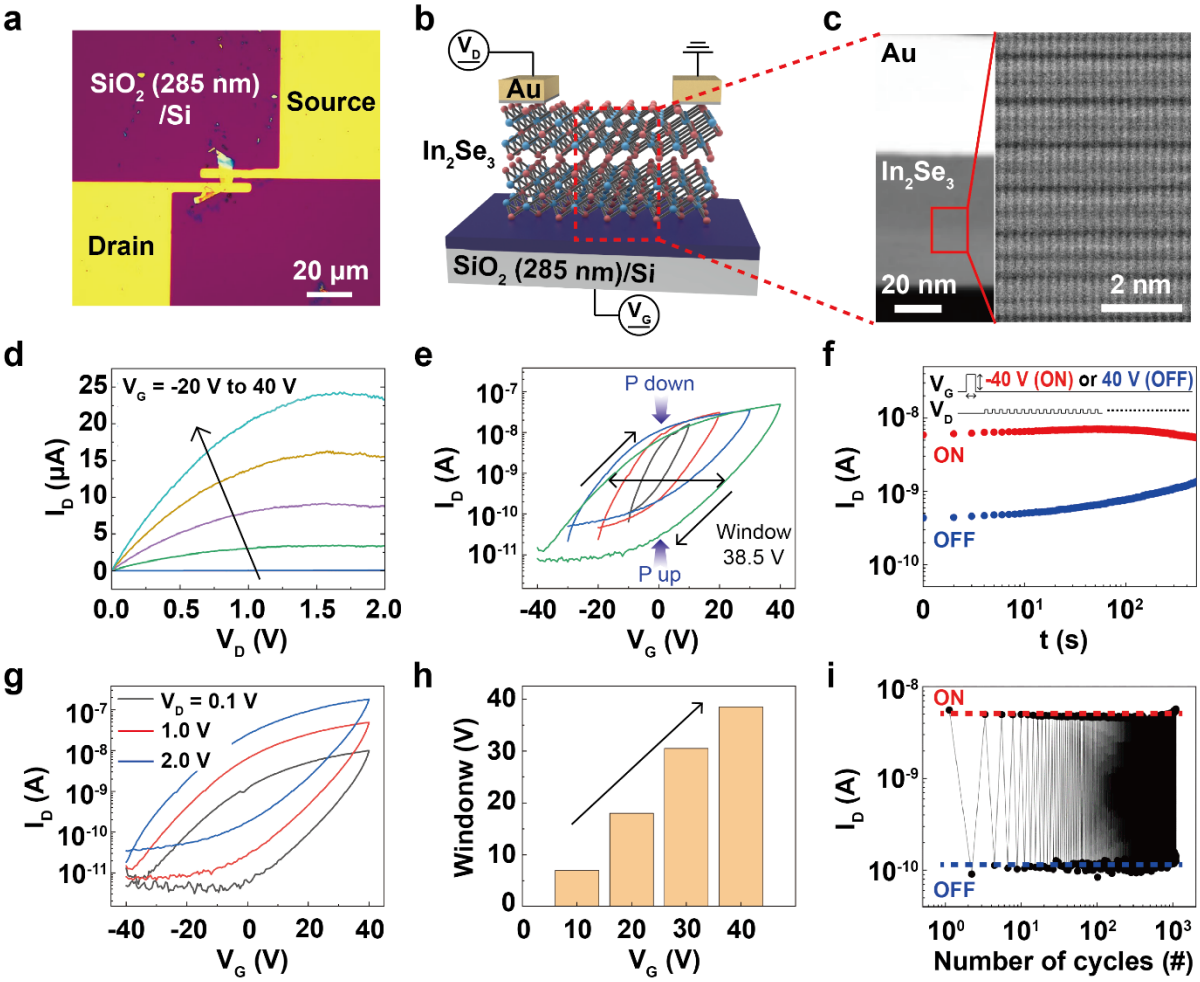

Figure 2. Electrical characteristics of α-In_2Se_3 FET devices at room temperature and high vacuum. a, Optical image and **b**, device schematic of the experimental α-In_2Se_3 FET device with source and drain electrodes of Au (50 nm)/Cr (5 nm). **c**, Cross-sectional ADF-STEM images of the experimental α-In_2Se_3 FET device. **d**, A representative I_D-V_D under different V_G **e**, I_D-V_G characteristics under different V_G sweep range (from ±10 to ±40 V). **f**, Retention characteristics of α-In_2Se_3 FET device. **g**, A representative I_D-V_G under different V_D. **h**, Hysteresis memory window under different V_G sweep range. **i**, Robust endurance characteristics of α-In_2Se_3 FET device for 1,000 write/erase cycles, without the degradation of ON and OFF states.

Figure 3

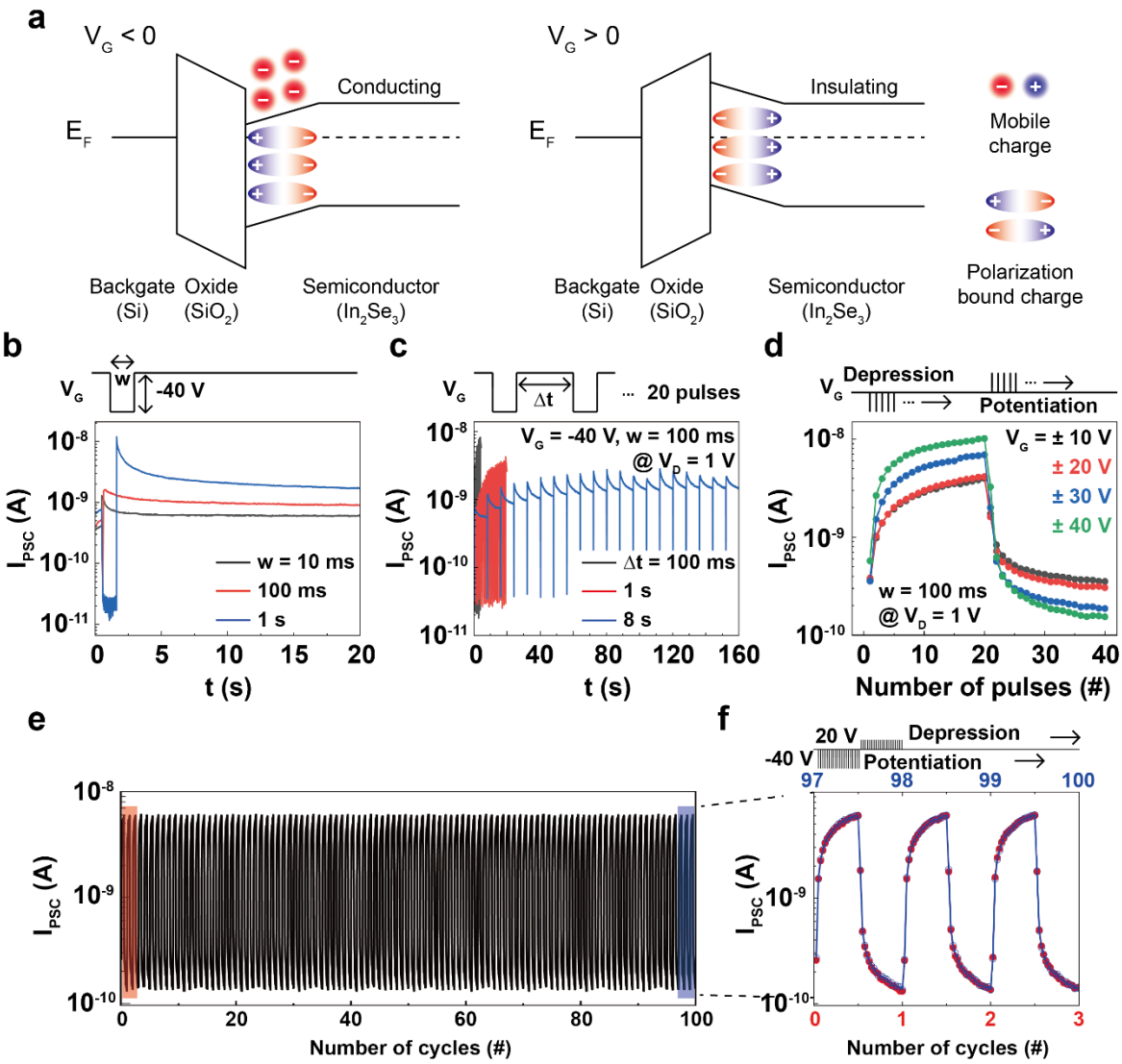

Figure 3. Working mechanism and artificial neuromorphic device characteristics of α-In_2Se_3 FET device. a, Schematics of the band diagrams under $V_G < 0$ (polarization (P) down) and $V_G > 0$ (P up) states. **b**, The post-synaptic current (PSC) responses at $V_D = 1$ V triggered by different pulse width (w) of 10 ms (black), 100 ms (red), and 1 s (blue). **c**, The PSC responses at $V_D = 1$ V triggered by 20 repeated potentiating pulses of V_G = -40 V for 100 ms with different interval timing (Δt) of 100 ms (black), 1 s (red), and 8 s (blue). **d**, LTP and LTD of PSC with different pulse amplitudes of V_G ranging from ±10 V to ±40 V with w of 100 ms. The number of potentiation and depression

pulses is 20. V_D and w are set as 1 V and 100 ms. **e**, Repetitive transitions of the LTP/LTD of PSC for the α-In_2Se_3 FET device for 100 cycles. **f**, Red and blue circles correspond to the first and last three cycles, respectively, for repetitive LTP/LTD of PSC in **e**.

Figure 4

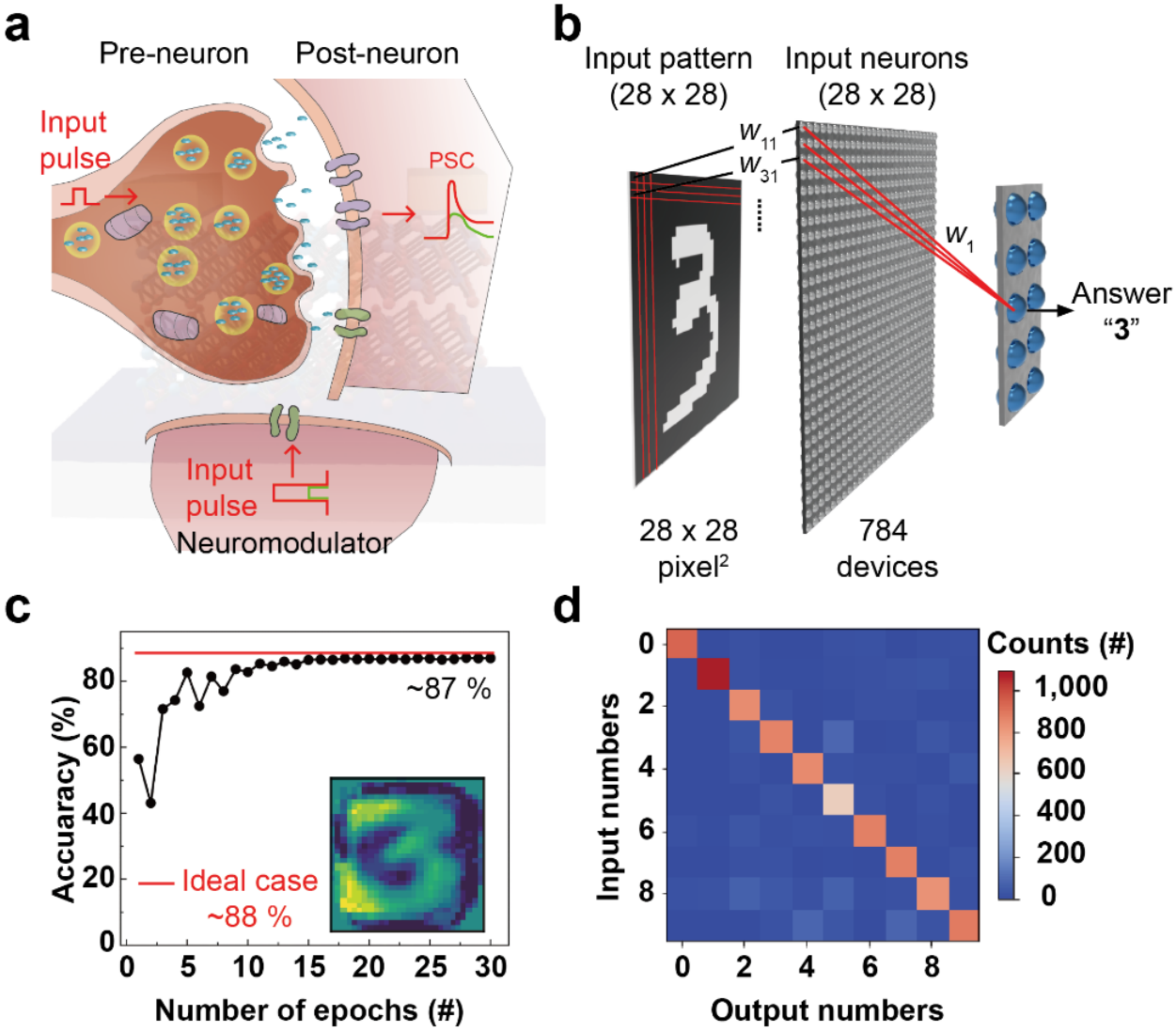

Figure 4. MNIST pattern recognition simulation. a, The illustration of tri-synaptic structures. **b**, Schematic representation of a single-layer neural network for the MNIST pattern recognition process where 28 × 28 (786) input neurons with binary brightness (black and white) and 10 output neurons are fully connected by 28 × 28 × 10 (7,860) artificial synapses to be selected as designated class among 10 digit classes (0, 1, 2, …, 9). **c**, MNIST pattern recognition accuracy for 30 learning epochs. The red line represents the pattern recognition accuracy for ideal case. The inset shows the

28 × 28 contour image of the digit 3 after 30th epochs. **d**, The confusion matrix for 10,000 test images after the training process where the row indicates recognited classes, and the column indicates the actual classes.