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In_2Se_3 Synthesized by the FWF Method for Neuromorphic Computing

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The development of next-generation in-memory and neuromorphic computing can be realized with memory transistors based on 2D ferroelectric semiconductors. Among these, In_2Se_3 is the interesting since it possesses ferroelectricity in 2D quintuple layers. Synthesis of large amounts of In_2Se_3 crystals with the desired phase, however, has not been previously achieved. Here, the gram-scale synthesis of α-In_2Se_3 crystals using a flash-within-flash Joule heating method is demonstrated. This approach allows the synthesis of single-phase α-In_2Se_3 crystals regardless of the conductance of precursors in the inner tube and enables the synthesis of gram-scale quantities of α-In_2Se_3 crystals. Then, α-In_2Se_3 flakes are fabricated and used as a 2D ferroelectric semiconductor FET artificial synaptic device platform. By modulating the degree of polarization in α-In_2Se_3 flakes according to the gate electrical pulses, these devices exhibit distinct essential synaptic behaviors. Their synaptic performance shows excellent and robust reliability under repeated electrical pulses. Finally, it is demonstrated that the synaptic devices achieve an estimated learning accuracy of up to ≈87% for Modified National Institute of Standards and Technology patterns in a single-layer neural network system.

1. Introduction

Two-dimensional (2D) semiconductors with inherent polarization based on homostructures or heterostructures offer numerous advantages for distinct electronic applications, including diode,[1–4] photodiode,[5–7] ferroelectric field-effect transistor (Fe-FET),[8–11] in-memory computing,[12–14] and neuromorphic applications.[15–17] Due to their atomically thin thickness and inherent polarization properties, 2D Fe-FETs have the potential for higher integration density in electronic circuits and integrated logic and memory functions with low energy consumption, surpassing conventional von Neumann computing architectures.[18] Among the various reported 2D ferroelectric materials, such as In_2Se_3,[19] SnSe,[20] $MoTe_2$,[21] and SnS,[22] α-In_2Se_3 stands out with its appropriate bandgap (1.39 eV), and room-temperature out-of-plane and in-plane ferroelectric characteristics with a Curie temperature >200 °C, even down to the monolayer limit.[19]

Bottom-up synthetic methods, such as chemical-vapor deposition (CVD),[23] physical vapor deposition (PVD),[24] molecular beam epitaxy (MBE),[12] and pulsed-laser deposition (PLD),[25] have been used to synthesize atomically thin In_2Se_3 layers. For

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example, the CVD methods have been intensively investigated and demonstrated to grow large-area 2D In_2Se_3 films. Due to complicated polymorphism and the low phase-transition temperature between In_2Se_3 phases, however, it is difficult to synthesize pure-phase In_2Se_3 films.[26] In addition, bottom-up strategies for producing high-quality In_2Se_3 are often restricted to ultrasmall amounts. Recently, flash Joule heating (FJH) has been demonstrated as an effective method for producing gram-scale flash graphene from various carbon feedstocks,[27–30] kilogram scales in automated FJH laboratory systems,[31] and ton-scales in industry (www.universalmatter.com). Contrary to conventional bottom-up synthetic methods, FJH provides short electrical pulses of high energy density followed by rapid cooling that can generate products within milliseconds to seconds with high energy efficiency.[27] Moreover, FJH can be used for phase control of transition metal dichalcogenides (TMD),[32,33] heteroatom doped-graphene,[34] and turbostratic-layered 2D materials.[35] A significant limitation of FJH, however, is that for Joule heating to occur, the precursors should have a resistivity below a certain level (0.5 – 30 Ω). To solve this requirement, carbon additives or metal powders are often mixed into the precursors to generate a conducting path for electrical current, facilitating the reaction.[27] These additives can generate undesired byproducts, often the metal(0) or metal carbide.[36]

To overcome this limitation of FJH, our group recently developed a method called flash-within-flash Joule heating (FWF) to achieve indirect heating, enabling non-conductive precursors to undergo flashing through thermal conduction.[37] In this study, we present the synthesis of pure α-In_2Se_3 crystals by employing the FWF approach. This method allows us to produce single-phase α-In_2Se_3 crystals even if the precursor in the inner tube is non-conductive, thereby generating α-In_2Se_3 crystals on the gram-scale. Moreover, we fabricated and used ferroelectric semiconductor FET (FS-FET) devices with α-In_2Se_3 flakes as a 2D FS-FET artificial synaptic device platform. They exhibit distinct essential synaptic behaviors through careful modulation of the degree of polarization of the α-In_2Se_3 flakes, depending on the gate-electrical stimulus. In addition, their synaptic performance shows excellent and robust reliability under repeated electrical pulses. Finally, we demonstrated that the estimated learning accuracy of our synaptic devices is up to ≈87% for Modified National Institute of Standards and Technology (MNIST) patterns in a single-layer neural network system.

2. FWF Process and α-In_2Se_3 Crystals Characterization

Figure 1a is a schematic diagram of the FWF synthesis process as an indirect Joule heating mechanism that allows the feedstocks of indium (In) pellets and selenium (Se) powder to be reacted rapidly within 3 s. The reaction occurs in two quartz tubes: an outer flashing vessel filled with a conductive material, such as metallurgical coke, and an inner flashing vessel that contains the feedstocks of In (0) and Se (0). The inner flashing vessel was filled by In pellets and Se powder with molar ratio of 1:3, and we applied a flashing voltage of 300 V to the outer vessel to generate the Joule heating process. Figure 1b exhibits the current profiles during the flashing process in the FWF system. While the current passes through the conductive feedstocks in the outer vessel, resistive Joule heating generates a high temperature of >2000 °C in the outer vessel, as measured by an infrared sensor (Figure S1, Supporting Information). Since the discharge is pulsed at different duty cycles of 10%, 20%, and 50% (Figure S2, Supporting Information), a constant reaction temperature, pressure, and volume is not achieved during the flashing, leading to a kinetically assisted synthetic process during the FWF method. Based on a Gibbs free energy calculation, an energy favorable reaction can be achieved in the range of the temperature during the flashing, meaning that the synthesis of In_2Se_3 is feasible by the FWF method (Figure S3, Supporting Information). Moreover, the metallurgical coke in the outer vessel is converted into the turbostratic flash graphene after the FWF reaction, consistent with the gram-scale graphene synthesis studies (Figure S4, Supporting Information).[27,31]

To verify the physical characteristics of the products from FWF synthesis, we conducted transmission electron microscopy (TEM), X-ray diffraction (XRD), X-ray photoelectron spectroscopy (XPS), Raman spectroscopy, and piezoelectric force microscopy (PFM) measurements. Figure 1c shows annular dark-field scanning transmission electron microscopy (ADF-STEM) images of α-In_2Se_3 crystals with highly crystalline structure, and corresponding Fourier transform shown in the inset of Figure 1c. In addition, the elemental compositions of the flakes are investigated by energy dispersive spectrometer (EDS) mapping (Figure S5, Supporting Information). From the results, the synthesized flakes are confirmed to be composed of pure In and Se. Figure 1d exhibits the XRD pattern of the as-prepared powders. All the diffraction peaks correspond to the hexagonal α-In_2Se_3 phase (DB card number: 00-034-1279) with hexagonal $P6_3mc$ crystalline structure. In the Raman spectra shown in Figure 1e, the representative A_1^1, E^4, and A_1^2 vibrational modes are observed at 105, 181, and 193 cm^{-1}, respectively, confirming α-phase In_2Se_3 flakes.[38] XPS was also conducted to confirm the atomic composition of the flakes (Figure 1f). From the full-scan XPS spectrum (Figure S6, Supporting Information), the spectral characteristic peaks clearly indicate the formation of In_2Se_3. The 3*d* doublets of In and Se clearly demonstrate the chemical valence of In and Se in In_2Se_3 flakes. The negligible carbon and oxygen signals of are presumably from the atmosphere. The PFM data is presented in the Supporting Information and shows that typical piezoelectric response was observed with different amplitudes and phases according to their polarization directions (Figures S7 and S8, Supporting Information). Moreover, when scaling up to gram-scale the α-In_2Se_3 retains its high purity and single-phase structure while the synthesis time remains within 3 s (Figure S9, Supporting Information). Hence, the gram-scale synthesis of α-In_2Se_3 crystals by the FWF method was confirmed to afford a single phase with high crystallinity.

3. Electrical Characteristics of α-In_2Se_3 Synthesized by the FWF Method

To investigate the electrical characteristics of as-prepared α-In_2Se_3 flakes by FWF, a FET with α-In_2Se_3 flakes was

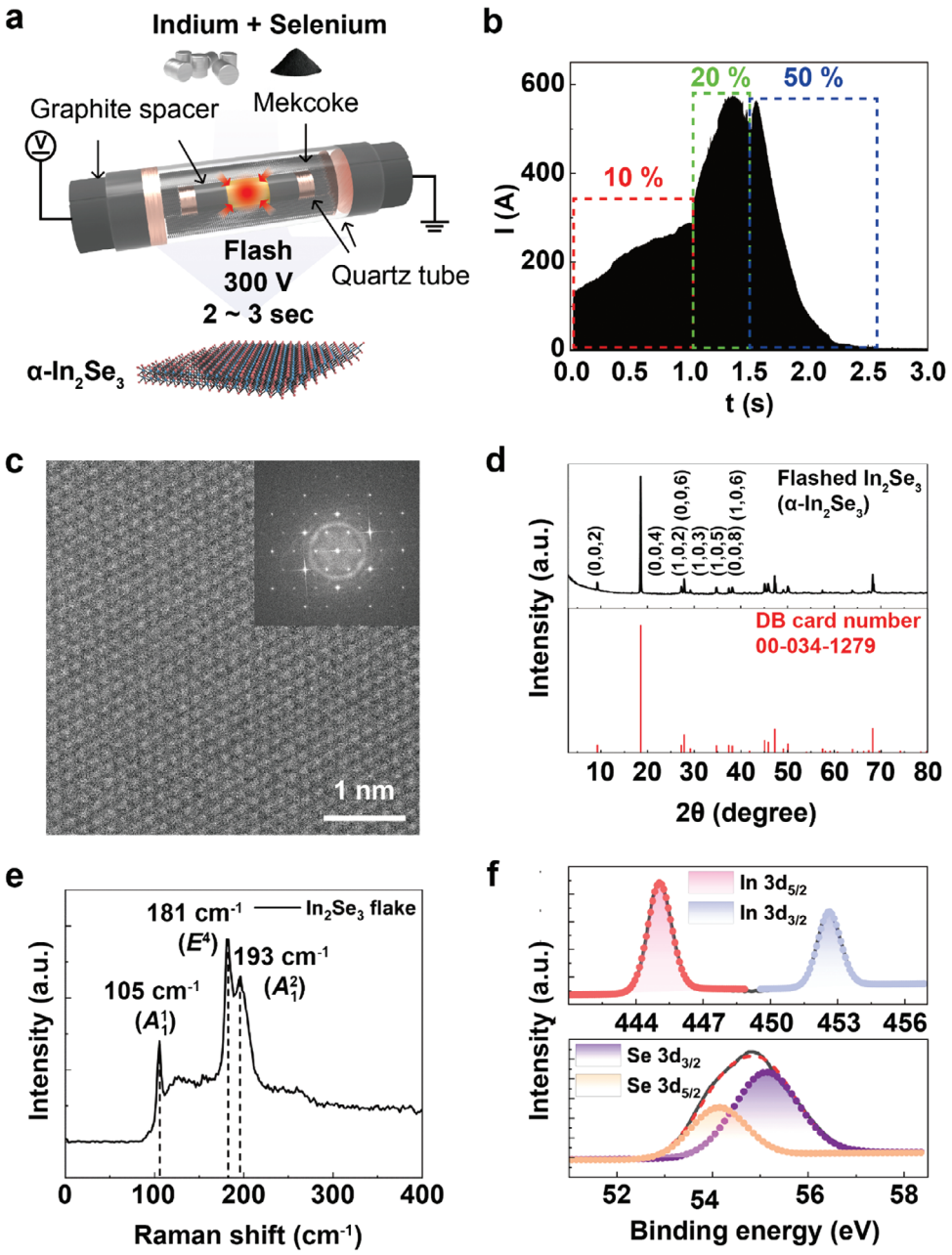

Figure 1. A α-In_2Se_3 synthesis by flash-within-flash Joule heating (FWF) and materials characteristics. a) A schematic of FWF with the precursors of In metal pellets and Se powder forming α-In_2Se_3. b) The current profile of 300 V FWF reaction. The dashed boxes indicate the regions of different duty cycles (10% (red), 20% (green), and 50% (blue)). c) Annular dark field STEM image and Fourier transform (inset) of α-In_2Se_3 powder d) XRD spectra of α-In_2Se_3 with R3m crystalline structure. e) Raman spectrum of α-In_2Se_3 with typical Raman peaks of 105, 181, and 193 cm^{-1}. f) XPS of α-In_2Se_3 for In (top) and Se (bottom) atoms.

fabricated. **Figure** 2a,b exhibit an optical microscope image and schematic of the α-In_2Se_3 FET device, where the FET device consists of a SiO_2 (285 nm)/Si (heavily p-doped) substrate as a backgate configuration, 2D α-In_2Se_3 flakes as the ferroelectric semiconductor channel and 10 nm Ti/50 nm Au as source/drain electrode contacts. The details of the device fabrication procedure are discussed in the Methods section and Supplementary Information (Figure S10, Supporting Information). As shown in Figure 2c, the individual layers of α-In_2Se_3 are distinct in the cross-sectional high-resolution ADF-STEM image, indicating that the α-In_2Se_3 FET devices are cleanly fabricated without noticeable damage of the interlayer and electrode contacts. Figure 2d,g exhibit representative output (drain voltage (V_D)-drain current (I_D) characteristics depending on various gate voltage (V_G)) and transfer curve (V_G-I_D characteristics depending on various V_D) for the α-In_2Se_3 FET device, respectively, and show typical *n*-type semiconducting behavior (Figure S11, Supporting Information) with a channel current ON/OFF ratio of > 10^4.[8]

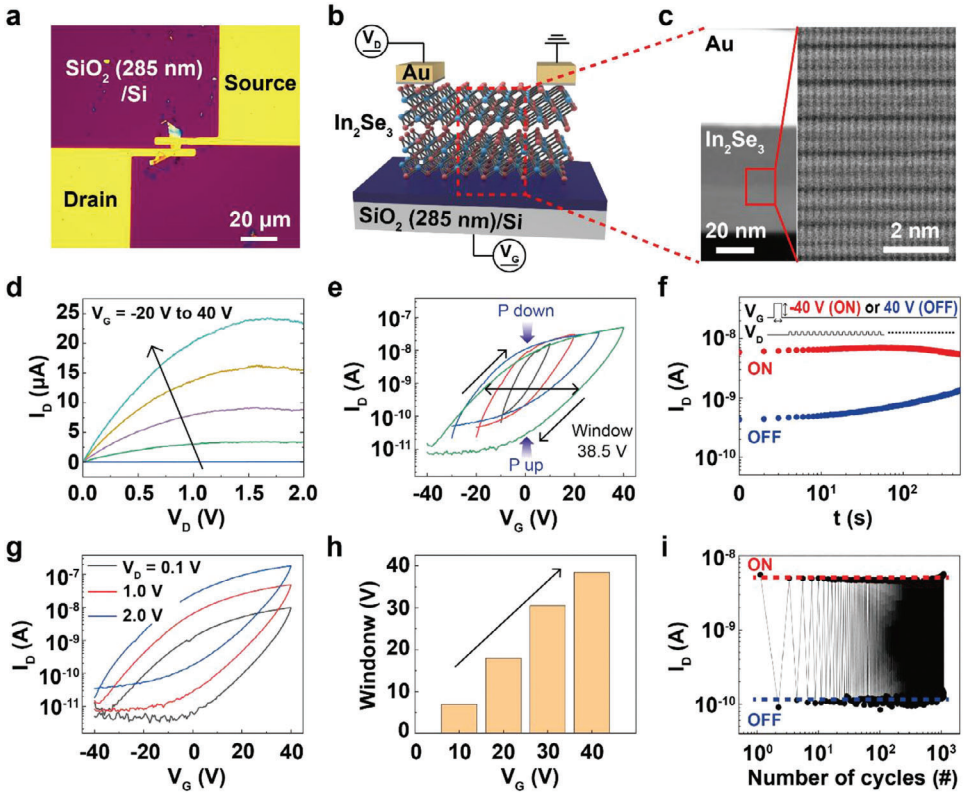

Figure 2. Electrical characteristics of α-In_2Se_3 FET devices at room temperature and high vacuum. a) Optical image and b) device schematic of the experimental α-In_2Se_3 FET device with source and drain electrodes of Au (50 nm)/Cr (5 nm). c) Cross-sectional ADF-STEM images of the experimental α-In_2Se_3 FET device. d) A representative I_D-V_D under different V_G e) I_D-V_G characteristics under different V_G sweep range (from ±10 to ±40 V). f) Retention characteristics of α-In_2Se_3 FET device. g) A representative I_D-V_G under different V_D. h) Hysteresis memory window under different V_G sweep range. i) Robust endurance characteristics of α-In_2Se_3 FET device for 1000 write/erase cycles, without the degradation of ON and OFF states.

Since the α-In_2Se_3 is highly light sensitive, we measured the electrical characteristics under dark conditions (Figures S12 and S13, Supporting Information). Moreover, the gate double sweep from -40 to 40 V for 100 cycles was conducted to investigate the device stability under repetitive electric stimuli (Figure S14, Supporting Information). After 100 cycles of electrical stimuli, the transfer curve of the 100th sweep is almost identical with that of 1st sweep, suggesting that the devices are very stable and robust under repeated electrical excitation. In addition, a large clockwise hysteresis is observed when the V_G is double swept between -40 and 40 V at a fixed V_D of 0.1 (black), 1.0 (red), and 2.0 V (blue) in Figure 2e, indicating that the device can exhibit a memory operation under V_G sweep.[8,13,15,39] Note that the transistor performance parameters including mobility, subthreshold swing, subthreshold voltage, and Schottky barrier height are given in Supporting Information (Figures S15–S18, Supporting Information). In addition, the hysteresis memory window can be tuned by using different gate sweep ranges (Figure 2h). When the gate sweep range becomes larger, the hysteresis window can be larger from 7.5 V under V_G sweep of -10 to 10 V to 38.5 V under V_G sweep of -40 to 40 V (Figure 2e), indicating that the polarization can be precisely controlled by adjusting the electric field. This results because the degree of polarization of In_2Se_3 can be stronger when the gate electric field is increased, leading to larger hysteresis memory window. Therefore, the device can exhibit two distinct electrical states after V_G is turned off, i.e., ON current state (ON) and OFF current state (OFF). The ratio between the two electrical states is $\approx 10^2$, indicative of a large dynamic range. Figure 2f exhibits a retention test for 5×10^2 s; however, the ON and OFF states were degraded after 10^2 s. Since the electron transfer direction and inherent polarization direction are perpendicular to each other, the mobile charge can disrupt the polarization direction, leading to degradation of the ON and OFF states.[40,41] Figure 2i exhibits an endurance test of our device by executing 10^3 repetitive pulse schemes (Figure S19, Supporting Information) with ON-OFF ratio of $< 10^2$. Unlike the retention test, the endurance characteristics were stable and robust for 10^3 cycles, so the device could be operated with stability under repetitive writing and erasing.

4. Ferroelectric Switching Mechanism

To understand the hysteresis phenomenon in α-In_2Se_3 FET devices, proposed energy-band diagrams for the two polarization states (up and down) are sketched after $V_G < 0$ or $V_G > 0$ was applied (**Figure 3a**). Note that the bandgap of α-In_2Se_3 can be changed from 1.64 to 1.44 eV when its thickness increases,[42] however, its ferroelectricity is only slightly changed upon varying the thickness.[43,44] The major charge transport mechanism in an In_2Se_3 FET device is Schottky emission, and when the

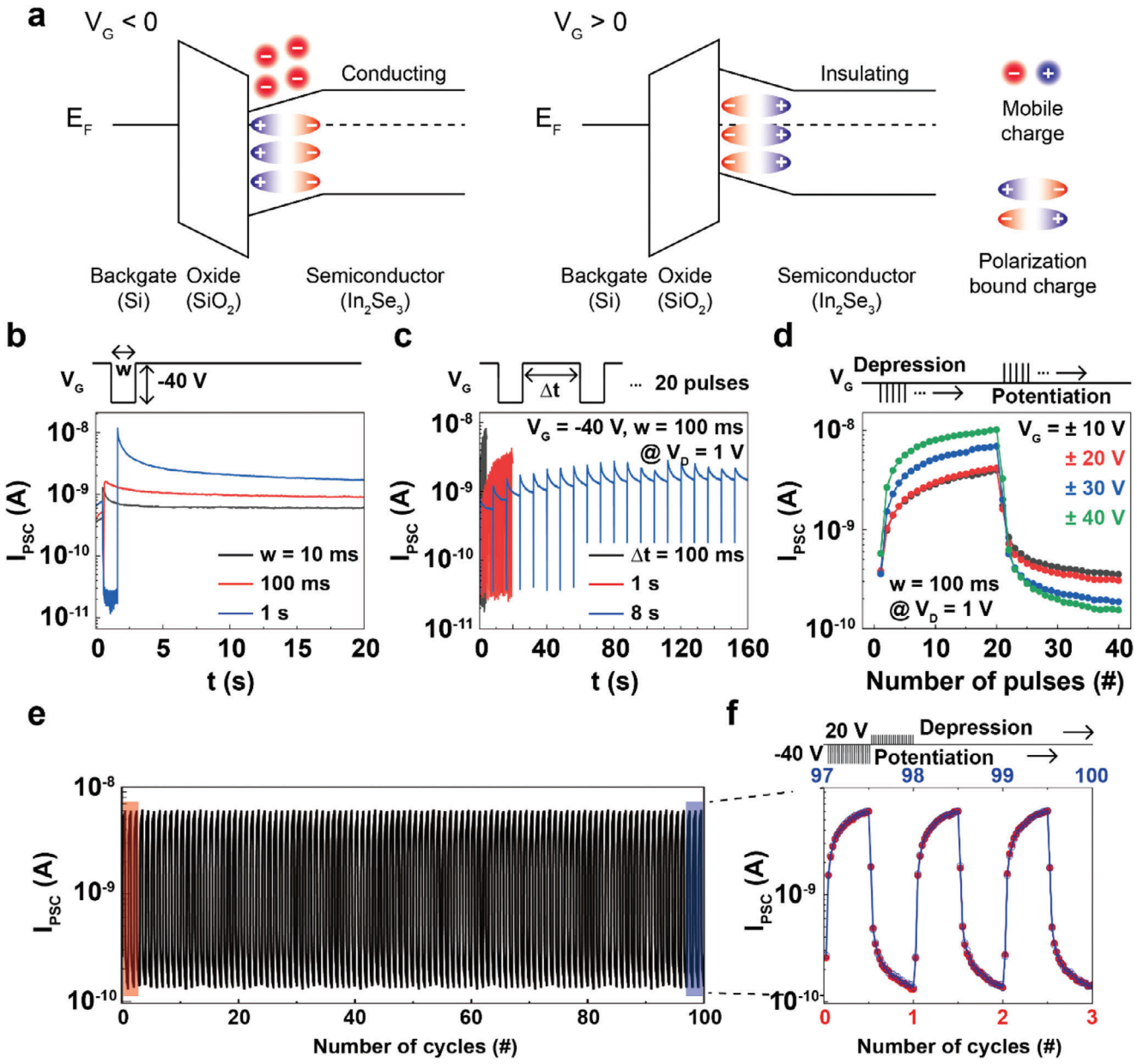

Figure 3. Working mechanism and artificial neuromorphic device characteristics of α-In_2Se_3 FET device. a) Schematics of the band diagrams under V_G < 0 (polarization (P) down) and V_G > 0 (P up) states. b) The post-synaptic current (PSC) responses at V_D = 1 V triggered by different pulse width (w) of 10 ms (black), 100 ms (red), and 1 s (blue). c) The PSC responses at V_D = 1 V triggered by 20 repeated potentiating pulses of V_G = -40 V for 100 ms with different interval timing (Δt) of 100 ms (black), 1 s (red), and 8 s (blue). d) LTP and LTD of PSC with different pulse amplitudes of V_G ranging from ±10 V to ±40 V with w of 100 ms. The number of potentiation and depression pulses is 20. V_D and w are set as 1 V and 100 ms. e) Repetitive transitions of the LTP/LTD of PSC for the α-In_2Se_3 FET device for 100 cycles. f) Red and blue circles correspond to the first and last three cycles, respectively, for repetitive LTP/LTD of PSC in e.

I_D-V_G characteristics are converted to $\ln(I_D)$ versus $V_G^{1/2}$, the converted graph exhibits a linear relationship (Figure S20, Supporting Information), meaning that the charge transport mechanism is indeed Schottky emission in the ON current regime. When a high negative V_G was applied, the polarization in α-In_2Se_3 was poled in the downward direction.[8,19] Consequently, positive-bound charges near the interface between α-In_2Se_3 and SiO_2 are produced, leading to a downshift of the energy band. In contrast, when a high positive V_G was applied, the polarization of α-In_2Se_3 was switched to the upward direction, inducing that negative-bound charges near the interface between α-In_2Se_3 and SiO_2 is produced and energy band of α-In_2Se_3 can be downshifted.[8,19] The polarization characteristics can be maintained even when the V_G is turned off due to the ferroelectric characteristics of α-In_2Se_3. Therefore, the α-In_2Se_3 FET device can exhibit non-volatile memory characteristics with ON and OFF states after V_G < 0 and V_G > 0, respectively. The details are discussed in Experimental Section.

5. Synaptic Behavior of α-In_2Se_3 Synthesized by the FWF Method

The α-In_2Se_3 FS-FET artificial synapse can implement two essential synaptic functions distinguished by a temporal or persistent change in the synaptic weight: (i) short-term plasticity (STP) and (ii) long-term plasticity (LTP). Figure 3b shows the post-synaptic current (I_{PSC}) changes over time generated by different single presynaptic pulses of V_G = -40 V with pulse widths (w) of 10 ms (black), 100 ms (red), and 1 s (blue) at V_D = 1 V. When the shorter w (V_G = -40 V for 10 ms) was applied to the preneuron (gate electrode), the I_{PSC} was temporally changed, i.e., its value returned to the original one. This I_{PSC} behavior is analogous to the STP of a biological synapse, which is excited for only a short period. In contrast, when the longer w (V_G = -40 V for 1 s) was applied to the preneuron, the I_{PSC} increased abruptly from 4.53×10^{-10} to 1.61×10^{-9} A, and then regained their electrical state for a longer period. Note that the temporal current drop before increasing the current originates from the gate-electric-field effect. This I_{PSC} behavior is analogous to LTP that represents memory consolidation in the brain. The V_G pulses for increasing I_{PSC} are called the potentiating pulse.

A longer V_G (-40 V for 1 s) can sufficiently move more charge around to interfaces in the longer time which can hold the polarization better in the α-In_2Se_3 layer compared with a shorter V_G (-40 V for 10 ms). Therefore, the electrons can accumulate at the interface between the α-In_2Se_3 and SiO_2 layer, increasing the electrical current states and retaining it for a long time. LTP can be mimicked because the accumulated electrons at the interface are retained to some extent owing to the remnant upward polarization. Considering the similarity of the operation to a biological synaptic cleft, the upward polarization degree can be regarded as the quantity of the neurotransmitters released and the concentration of the Ca^{2+} influx into the axon terminal of the preneuron, respectively.[45]

The synaptic weight can also be controlled by changing the number of preneuron voltage pulses applied in a given time; that is, the degree of the I_{PSC} increases can be affected by the time interval (Δt) between two potentiating pulses. Figure 3c shows the I_{PSC} changes for 20 repeated pulses (V_G = -40 V for 100 ms) depending on different Δt (0.1 (black), 1 (red), and 8 s (blue), respectively). A shorter Δt (0.1 s) led to a larger and more rapid increase in the I_{PSC}. This results because the potentiating pulses with a shorter Δt further induced the upward domain of polarization before the postsynaptic responses to the previous pulse were completely attenuated, leading to strengthen and retaining the degree of polarization in α-In_2Se_3 crystals. In contrast, the longer Δt (8 s) could fully attenuate the response; hence the final I_{PSC} was barely changed. This Δt dependency on the I_{PSC} is like the phenomenon of temporal summation of the signal propagation that occurs when the input graded potentials from one biological preneuron are close together over a given time. This is regarded as one of the main features of the spike rate-dependent plasticity (SRDP).[46] Since higher absolute values of input pulses can further change the direction of polarization, the dynamic range of I_{PSC} can also be increased as the V_G increased from ±10 to ±40 V (Figure S21, Supporting Information).

Figure 3d shows the gradual LTP and long-term depression (LTD) of I_{PSC} depending on the continuous potentiating and depressing input pulse trains. When the polarity of the presynaptic pulse is changed from negative to positive, the direction of polarization is changed to the opposite, which can repel the accumulated electrons and deplete the interfacial region. Consequently, the I_{PSC} gradually decreases during the positive depressing input pulse train. This gradual I_{PSC} reduction is analogous to the LTD of a biological synapse.[43] For practical and robust neuromorphic device applications, stable synaptic functions under repeated pulse cycles are essential. Figure 3e shows the repetitive transitions between LTP/LTD functions over 4000 continuous input pulses. The number of presynaptic pulses for one cycle was 40, each consisting of 20 potentiating pulses (V_G = -40 V for 100 ms) and 20 depressing pulses (V_G = 20 V for 100 ms), demonstrating stable repetitive LTP/LTD functions over the 4000 electrical pulses. Furthermore, the I_{PSC} values for the first (red) and last three cycles (blue) were almost identical (Figure 3f). These stable synaptic functions under repeated pulse cycles were demonstrated under V_G = ±10, ±20, and ±30 V, respectively, where the electrical characteristics are stable and robust regardless of the operating voltage amplitudes (Figures S22–S24, Supporting Information). This indicates the reproducibility and robust control of the synaptic weight with very stable operation even over 4000 electrical pulses. Compared to previous studies, our In_2Se_3 FET devices exhibited good ON/OFF ratio and linearity in the LTP/LTD curves, which can mainly determine the pattern recognition accuracies.[47–50] The details of comparison of neuromorphic performance are shown in Supporting Information (Table S1, Supporting Information).

6. MNIST Pattern Recognition Simulation

To evaluate the learning capability of the α-In_2Se_3 FS-FET device (**Figure 4a**) to be a constituent as a synaptic weight element in tri-synaptic artificial neural network for neuromorphic applications, we prepared an unstructured data set and single-layer neural network platform to adjust the analog conductance of the device and to update the synaptic weights (Figure 4b). The details of MNIST pattern recognition simulation are discussed in Supporting Information (Notes S1 and S2, and Figure S25, Supporting Information). We simulated the training and test process using 20-level analog switching characteristics of the α-In_2Se_3 FS-FET device in the influence of different gate voltage (10, 20, 30, and 40 V) for the conventional binary MNIST digit image set (60000 training and 10000 test set).[51] Here, the test set was prepared differently from the training set to identify the availability of the formed 10 × 28 × 28 synaptic weight map for recognizing the correct output class. The 10-class (0, 1, 2, ..., 9) MNIST datasets contain images of 28 × 28 pixels represented by binary resolution and are further determined by pixel brightness (black and white pixels). The training principle of the neuromorphic perceptron process is provided in the Note S1 (Supporting Information). Figure 4c shows classification accuracy during 30 training processes at gate voltage of 10 V. As the training epoch increases, the accuracy value is evolved to converge to ≈87%, which is near the ideal single-layer accuracy of ≈88% using numerical weight values excluding device parameters. The classification accuracy for different operating voltages (V_G = 20, 30, and 40 V) is 86.77, 86.36, and 86.02%, respectively (Figure S26, Supporting Information).[51,52] Figure 4d shows the confusion matrix of

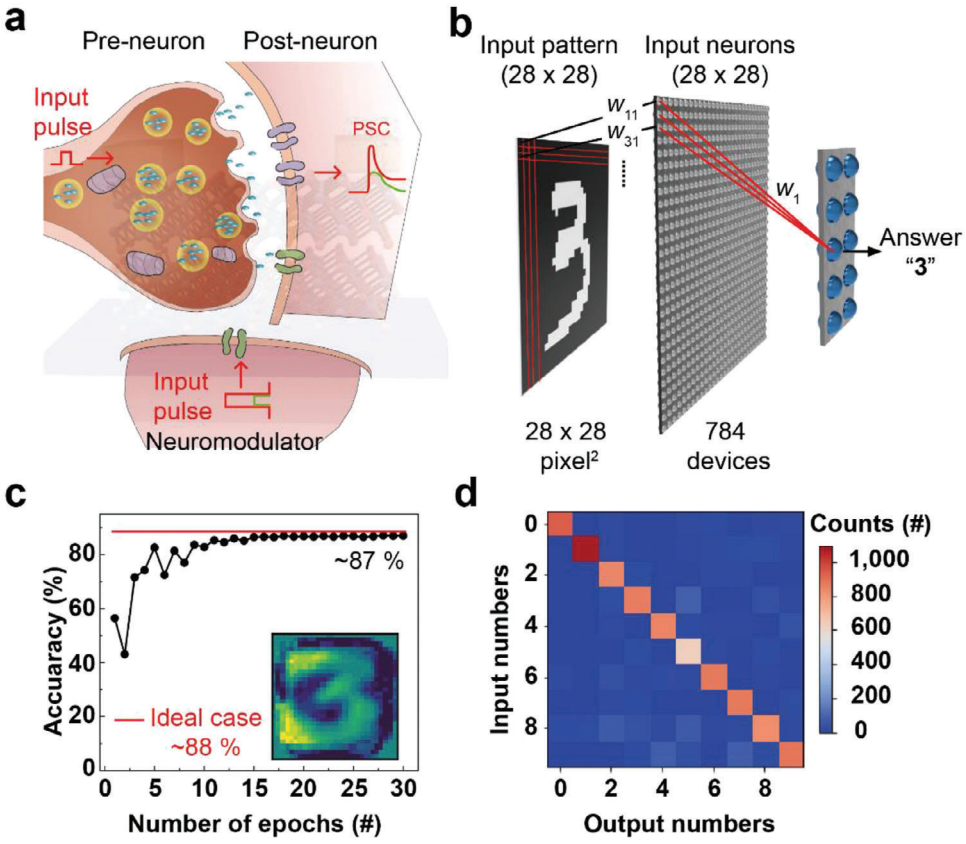

Figure 4. MNIST pattern recognition simulation. a) The illustration of tri-synaptic structures. b) Schematic representation of a single-layer neural network for the MNIST pattern recognition process where 28 × 28 (786) input neurons with binary brightness (black and white) and 10 output neurons are fully connected by 784 × 10 (7860) artificial synapses to be selected as designated class among 10 digit classes (0, 1, 2, ..., 9). c) MNIST pattern recognition accuracy for 30 learning epochs. The red line represents the pattern recognition accuracy for ideal case. The inset shows the 28 × 28 contour image of the digit 3 after 30th epochs. d) The confusion matrix for 10000 test images after the training process where the row indicates recognited classes, and the column indicates the actual classes.

10 000 test images after the 30-training epoch at a gate voltage of 10 V. Here, the row indicates recognized classes, and the column indicates the actual classes. The ratio of summation of diagonal elements to the entire 10 000 images shows recognition accuracy of ≈87%. Based on these results, the single-neural network based on the α-In_2Se_3 FS-FET device properly and accurately performs the learning and recognition tasks.

7. Conclusion

In conclusion, highly crystalline and single-phase α-In_2Se_3 was successfully synthesized by the FWF reaction, and the materials characteristics were analyzed by XRD, XPS, EDS, TEM, and Raman analysis. Based on as-synthesized α-In_2Se_3 with single phase and high crystallinity, the α-In_2Se_3 synaptic devices were successfully fabricated. Diverse and well-defined synaptic functions, including STP, LTP/LTD, and SRDP, were demonstrated. In addition, the transitions between the LTP/LTD functions were stable under repeated pulse cycles regardless of operating voltage amplitude. Notably, the α-In_2Se_3 synaptic devices achieved up to ≈87% recognition accuracy for MNIST patterns, even in a single-layer neural network system. In order to check the possibilities of electronic applications and other applications, we investigated the energy band structure and ferroelectricity with the electrical and neuromorphic characteristics of α-In_2Se_3 as a representative. In this regard, the α-In_2Se_3 materials synthesized FWF can be realized in various scientific embodiments including solar cells, batteries, photocatalysis, thermoelectricity, as well as ferroelectricity.

8. Experimental Section

Materials Synthesis: In metal pellets (0.42 g) and Se powder (0.84 g) were placed inside the 8 mm quartz tube with graphite spacer and copper mesh at each end of the quartz tube. Only graphite spacers were in contact with the metal precursors. This tube is then placed inside the 15 mm quartz tube and is subsequently filled with metallurgical coke (5.0 g). The copper mesh and graphite spacer were also placed at each end of the outer quartz tube. The combined tubes were flash-Joule-heated using 300 V, and the products from FJH were collected without further purification and washing. For gram-scale synthesis, In metal pellet (0.84 g) and Se powder (2.15 g) were placed inside the 8 mm quartz tube with graphite spacer and copper mesh at each end of the quartz tube, and FWF system was made with the same procedure. The combined tubes were flash-Joule-heated using 260 V, and the products from FJH were collected without further purification and washing.

Material Characterization: Materials characterization of α-In_2Se_3 was carried out to investigate α-In_2Se_3, as a single-crystal semiconducting

and ferroelectric material, including STEM, Raman spectroscopy, XPS, and XRD. STEM images were collected on a FEI Titan Themis S/TEM system operating at 300 keV. The powder samples were prepared by drop-casting a 300-µL aliquot (1 mg of sample per 1 mL ethanol) on Cu/lacey carbon TEM grid (Ted Pella). The resultant grid was dried at 80 °C on a hotplate for 1 h with subsequent overnight vacuum drying. For cross-sectional TEM images, focused ion beam (FIB) cutting was performed with FEI Helios NanoLab 660 DualBeam system. The resultant FIB cross-section sample was attached to PELCO Cu half grids (Ted Pella) for further characterization under ADF-STEM. Raman spectra were obtained using a Renishaw Raman microscope (532 nm laser, 50× lens) with the exfoliated α-In_2Se_3 flakes on SiO_2/Si substrate. XPS were obtained using PHI Quantera SXM Scanning X-ray Microprobe with a base pressure of 5×10^{-9} Torr. All XPS spectra were corrected using carbon 1s (284.8 eV) peak as a reference. XRD spectra were collected using Rigaku SmartLab XRD with CuKα radiation from 2θ angle of 3° to 80° with the scan rate of 10 ° min^{-1}.

Ferroelectric Domain Imaging: The piezoelectric and ferroelectric properties of the α-In_2Se_3 flake were characterized by dual AC resonance tracking piezoresponse force microscopy (DART-PFM) using a commercial scanning probe microscope (MFP-3D Origin, Asylum Research). PFM was conducted with an AC bias voltage of 1 V using a conductive Pt/Ir-coated cantilever (PPP-EFM, Nanosensors) with a resonant frequency of ≈75 kHz and a spring constant of ≈2.68 N/m. Piezoresponse hysteresis loops of the α-In_2Se_3 flake were measured using the same cantilever while applying triangle-square waveforms sweeping the voltage pulses with a pulse width of 2.5 ms from 0, 9, 0, -9 to 0 V over 12 s accompanied by an AC bias voltage of 1 V to the tip at approximately the contact resonant frequency of ≈371 kHz. The amplitude and phase were measured when each DC bias voltage pulse was not applied (off-field mode or pulse DC mode) to exclude the electrostatic force between the tip and the sample.

Device Fabrication: The α-In_2Se_3 samples were prepared using typical mechanical exfoliation methods on SiO_2 (285 nm)/Si substrate, respectively. Briefly, as-prepared α-In_2Se_3 flakes were placed between two pieces of adhesive tape and then pulled off very carefully to make thinner layers of α-In_2Se_3. After repeating this process 5 times, the adhesive tape is pressed onto the SiO_2 substrate and gently rubbed for 2 min. And then the adhesive tape was gently pulled off. The thickness of the layers was estimated by optical contrast. Cross-sectional TEM was used to determine their thicknesses. To make electrical contact, conventional photolithography was used to make the source and drain patterns where the channel length is 3 µm, and 10 nm of Ti and 50 nm of Au metal were deposited by an electron beam evaporator under a pressure of ≈10^{-8} Torr and deposition rate of 2.0 Å s^{-1}. To remove the residual photoresist, the sample was immersed in an acetone bath for 6–12 h, and then the solution was gently blown by a stream of N_2 gas. Finally, to enhance the interfacial contact properties between metal/2D materials, the fabricated devices were stored for 6–12 h under vacuum (≈10^{-3} Torr) conditions. The processes used to fabricate the devices are schematically shown in Supplementary Information (Figure S8, Supporting Information).

Details of Ferroelectric Switching Mechanism: To understand the hysteresis phenomenon in an α-In_2Se_3 FET device, an energy-band diagram at the two polarization states (up and down) was employed after $V_G < 0$ or $V_G > 0$ was applied (Figure 3a). When the high negative V_G was applied, the inherent electric field in α-In_2Se_3 was formed in the downward direction. In contrast, when the high positive V_G was applied, the inherent electric field in α-In_2Se_3 was formed in the upward direction. Consequently, the positive-bound charges near the interface between α-In_2Se_3 and SiO_2 were produced, leading to energy band downshift. In contrast, the negative-bound charges near the interface between α-In_2Se_3 and SiO_2 were produced, leading to an energy band upshift. The polarization characteristics can be maintained even when the V_G was turned off due to the ferroelectric characteristics of α-In_2Se_3. Therefore, our α-In_2Se_3 FET device can exhibit non-volatile memory characteristics with ON and OFF states after $V_G < 0$ and $V_G > 0$, respectively. Note that it is known that multiple factors can result in clockwise gate hysteresis on transistors made from layered semiconductors, such as adsorption of water and oxygen molecules, interfacial charge states, and even intrinsic material defects. In this work, we verified that the hysteresis was attributed to the inherent ferroelectric characteristics of α-In_2Se_3 flakes based on a series of experimental conditions. The electrical measurements were conducted under high vacuum, where the contribution of surface adsorbates including water and oxygen can be excluded. Moreover, H_2 and O_2 plasma treatment was conducted on the SiO_2/Si substrate before α-In_2Se_3 flakes exfoliation to remove the dangling bond on the SiO_2 surface, thus this rules out the contribution of interface-trap-induced hysteresis. Therefore, we can verify that the clockwise hysteresis and memory characteristics of our devices originate from the inherent ferroelectricity of α-In_2Se_3.

Device Characterization: The electrical characteristics were measured with a semiconductor parameter analyzer (Agilent B1500A Semiconductor Device Analyzer) and a probe station system in the dark to avoid the generation of photo-excited electrons and holes in 2D materials. The source electrode was grounded, the drain voltage was applied by the drain electrode, and the Si substrate was used as the backgate electrode. The measurement was conducted under high vacuum condition (≈10^6 Torr)

Surface Treatment and Measurement Condition: It is known that multiple factors can result in clockwise gate hysteresis on transistors made from layered semiconductors, such as absorption of water and oxygen molecules, interfacial charge states, and even intrinsic material defects. In this work, we verify that the hysteresis is attributed to the inherent ferroelectric characteristics of α-In_2Se_3 flakes based on a series of experimental conditions. The electrical measurements were conducted under high vacuum, where the contribution of surface adsorbates including water and oxygen molecules can be minimized. Moreover, H_2 and O_2 plasma treatments were applied onto the SiO_2/Si substrate before α-In_2Se_3 flakes exfoliation to remove the dangling bonds on the SiO_2 surface, mitigating the contribution of interface-trap-induced hysteresis. Therefore, the clockwise hysteresis and memory characteristics of our devices originate from the inherent ferroelectricity of α-In_2Se_3.

MNIST Pattern Recognition Simulation: The MNIST pattern recognition simulation is based on the results of LTP and LTD in Figure 3 and was carried out to investigate the learning capability of the α-In_2Se_3 FET synaptic devices. This single-layer artificial neural network consists of 784 input neurons (28 × 28 pixels) and 10 output neurons with full connection by an individual synapse that has its own synaptic weight. The details of MNIST pattern recognition simulation are discussed in Note S1 (Supporting Information).

Flash Joule Heating Equipment: The flash Joule heating reactions were performed by a custom-built system using capacitor banks to deliver the flash. 48 Kemet ALS70A133QT500 capacitors, each rated at 13 mF and 500 V, were connected in parallel (624 mF total) and charged to the desired voltage. A variable frequency driver controlled the discharge intensity using pulse width modulation by using a duty cycle pattern operating at 1 kHz of 10% intensity for 1 s, followed by 20% for 0.5 s, and finally 50% for 5 s. It should be noted that almost all the voltage is used during the 10% and 20% duty cycle; the 50% duty cycle is to ensure all the voltage is discharged through the sample. The duty cycles, charging, and flashing operations were controlled by a custom LabVIEW program. The current discharged during flashing was measured using a Tamura L34S1T2D15 Hall effect sensor. The temperature was measured using a Micro-Epsilon CTRM1H1SF100-C3 pyrometer.

Supporting Information

Supporting Information is available from the Wiley Online Library or from the author.

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Conflict of Interest

Rice University own intellectual property (IP) surrounding the concepts in this manuscript. That IP is presently unlicensed.

Author Contributions

J.S. conceived with the device idea with C.H.C. and L.E., realized the demonstration of synthesizing In_2Se_3 materials by flash-within-flash Joule heating, conducted gram-scalability, XRD, XPS, Raman, electrical measurements, artificial neuromorphic measurements, and manuscript writing under the guidance of J.M.T.J.J. performed MNIST pattern recognition simulation. C.H.C. performed STEM and EDS characterization. L.E. managed the FJH system. P.S. aided Raman spectroscopy analysis. J.K. and L.W.M. performed the PFM measurement. Y.H. supervised C.H.C. in performing STEM and EDS characterization. J.M.T. supervised J.S. for all the process, guided J.S. in manuscript writing, and oversaw the entire project.

Data Availability Statement

The data that support the findings of this study are available in the supplementary material of this article.

Keywords

ferroelectricity, flash joule heating, flash-within-flash joule heating, neuromorphic applications, α-In_2Se_3

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